AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): A video signal judgment circuit ~~for detecting~~ arranged to detect the condition of a video signal compounding a picture signal and a synchronization signal ~~comprises~~ comprising:

a synchronization separation unit adapted to:

filter an inputted video signal with a low-pass filter having a cutoff frequency adjustable by a first control signal; and

separate a synchronization signal from the filtered video signal to output a pulsed synchronization detection signal~~,~~; and

a video signal judgment unit adapted to compare a detection signal formed on the basis of said synchronization detection signal with a judgment reference value that is adjustable by a second control signal and output a judgment signal based on the comparison; wherein

said video signal judgment unit includes:

a mono-multi circuit that undergoes mono-stable operation in response to said synchronization detection signal to output a mono-multi output signal having a pulse width regulated according to the period of cycle of said synchronization detection signal but stop said mono-multi output signal when no synchronization detection signal is fed in a predetermined period of time;

a smoothing circuit arranged to smooth said mono-multi output signal and to output the smoothed signal as said detection signal; and

a detection judgment comparison circuit including a first comparator arranged to compare said detection signal with a first judgment reference value adjusted by said second

control signal, said detection judgment comparison circuit adapted to output a judgment signal based on the comparison made;

Claim 2 (currently amended): The video signal judgment circuit according to claim 1, further including a logic circuit ~~for outputting~~ arranged to output said first and second control signals to adjust said cutoff frequency and judgment reference value upon receipt of an external instruction signal.

Claim 3 (original): The video signal judgment circuit according to claim 2, wherein each of said first and second control signals has a serial data form.

Claim 4 (currently amended): The video signal judgment circuit according to claim 1 ~~or claim 2~~, wherein said synchronization separation unit includes:

a low-pass filter having a variable resistor and a capacitor, the resistance of said resistor adjustable by said first control signal to regulate said cutoff frequency of said low-pass filter; and

a synchronization separation circuit ~~for separating~~ arranged to separate a synchronization signal from said video signal filtered out with said low-pass filter to output a pulsed synchronization detection signal.

Claim 5 (canceled).

Claim 6 (currently amended): The video signal judgment circuit according to claim ~~5~~ 1, wherein said mono-multi circuit ~~may~~ includes:

a capacitor chargeable through a charging resistor;

a switch element connected in parallel with said capacitor and switched on in accordance with said synchronization detection signal;

a comparator ~~for generating~~ arranged to generate a mono-multi output signal when the voltage of said capacitor exceeds a predetermined voltage; and

a time-limit control circuit ~~for stopping~~ arranged to stop said mono-multi output signal when no synchronization detection signal is fed in a predetermined period of time.

Claim 7 (currently amended): The video signal judgment circuit according to claim ~~5~~ 1, wherein said detection judgment comparison circuit further includes a second comparator ~~for comparing~~ arranged to compare said detection signal with a second judgment reference value higher than said first judgment reference value, said detection judgment comparison circuit adapted to output said judgment signal when said detection signal exceeds said first judgment reference value but is less than said second judgment reference value.

Claim 8 (original): The video signal judgment circuit according to claim 2, wherein said logic circuit and at least those circuits of said synchronization separation unit and said video signal judgment unit that are regulated by said first and second control signals of said logic circuit are integrated in a semiconductor IC.